Applicationguide, Performance test

This guide describes the usage of the performance test FPGA design and software. It is used to test the read and write speeds between a host system and the Spartan3 PCI Express Starter kit. This is done by repeatedly reading/writing a 32 bit register on the board, and measuring the time this takes.

Files used

The files used for this application can be found on CD1 in:

- FPGA Design: "*Source\FPGA_Design\IOControlDemo*"
- Windows device driver and applications: "*Source\Windows_Device_Drivers_and_Applications\Performancetest*"
- Linux device driver and applications: "*Source\Linux_Device_Drivers_and_Applications\Performancetest*"

The FPGA design

The *IOControlDemo* FPGA design is used. This provides two BAR modules, BAR0 which uses four registers to control the leds and pushbuttons on the Spartan3 PCI Express Starter kit, and BAR1 which is an 8 kB blockram.

The driver

The driver used here is the *Empty* driver, with functionality added to perform the driver-controlled tests, as described in journal 4.

The applications

Two applications are available, *perf_test*, which runs driver- and application-controlled tests, and *perf_test_mmap*, which runs driver-controlled and memory-mapped tests. For each test, the total time taken, the average time per read or write, and the effective and actual transfer rates are printed. The effective transfer rate is calculated as the amount of actual data (not including overhead) transferred per second, while the "actual" transfer rate is the total number of bytes transferred (data and overhead from the transaction layer).

Usage

Load the design into the FPGA (synthesize/implement if necessary), install the driver and run one of the applications.